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**North South University**

Department of Computer Science and Engineering

CSE332 Project: 20-bit single cycle CPU

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**Course:** CSE332

**Section:** 02

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**R-type Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Opcode | RS | RT | RD | Shift | Function |
| 3 bits | 3 bits | 3 bits | 3 bits | 4 bits | 4 bits |

**I-type Format:**

|  |  |  |  |
| --- | --- | --- | --- |
| Opcode | RS | RT | Immediate |
| 3 bits | 3 bits | 3 bits | 11 bits |

**J-type Format:**

|  |  |
| --- | --- |
| Opcode | Address |
| 3 bits | 17 bits |

**Opcode Table:**

|  |  |  |
| --- | --- | --- |
| Operation Type | Operations | Opcode |
| R-type | ADD, SUB, AND, OR, NOR, SLL, SRL, SLT | 000 |
| I-type | |  | | --- | | LW | | SW | | BEQ | | BNE | | |  | | --- | | 010 | | 001 | | 011 | | 111 | |
| J-type | Jump | 101 |

**Operation Table: (R-type)**

|  |  |
| --- | --- |
| ALU Operations | Function |
| ADD | 0111 |
| SUB | 0110 |
| AND | 0101 |
| OR | 0100 |
| NOR | 0011 |
| SLL | 0010 |
| SRL | 0001 |
| SLT | 1000 |

**Control Unit Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Ins.  Type | Op-  code | Reg-  Dst | ALU-  src | MemTo-  Reg | Reg-  Write | Mem-  Read | Mem-  Write | Branch | BEQ/BNE | ALUop1 | ALUop0 |
| R-type | 000 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| LW | 010 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| SW | 001 | X | 1 | X | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Bra-nch | 011 | X | 0 | X | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| BEQ/BNE | 111 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| J-type | 101 |  |  |  |  |  |  |  |  |  |  |